N- and P-Channel 30-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME4542 is the N- and P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- 30V/6.9A,$R_{DS(ON)}$=25mΩ@V_{GS}=10V (N-Ch)
- 30V/5.8A,$R_{DS(ON)}$=40mΩ@V_{GS}=4.5V (N-Ch)
- -30V/-6.1A,$R_{DS(ON)}$=35mΩ@V_{GS}=-10V (P-Ch)
- -30V/-5.1A, $R_{DS(ON)}$=58mΩ@ V_{GS}=-4.5V (P-Ch)
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

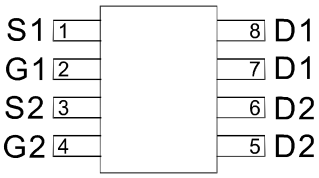
APPLICATIONS

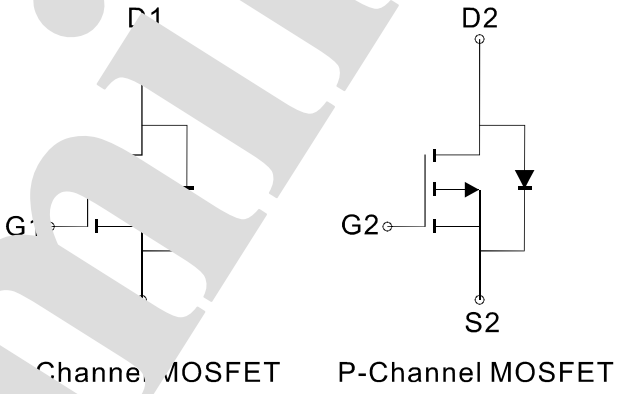
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC

PIN CONFIGURATION

(SOP-8)

Top View





Channel MOSFET P-Channel MOSFET

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DSS}	30	-30	V
Gate-Source Voltage		V_{GSS}	±20	±20	V
Continuous Drain Current(tJ=150℃)	T_A=25℃	I_D	6.9	-6.1	A
	T_A=70℃		5.5	-4.9	
Pulsed Drain Current		I_{DM}	30	-30	A
Continuous Source Current (Diode Conduction)		I_S	1.7	-1.7	A
Avalanche Energy with Single Pulse		EAS	10	20	mJ
Maximum Power Dissipation	T_A=25℃	P_D	2.0		W
	T_A=70℃		1.3		
Operating Junction Temperature		T_J	-55 to 150		℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	Steady 75	Steady 65	℃/W
			10sec 47	10sec 35	
Thermal Resistance-Junction to Case		$R_{\theta JC}$	44	30	℃/W

*The device mounted on 1in2 FR4 board with 2 oz copper

N- and P-Channel 30-V (D-S) MOSFET

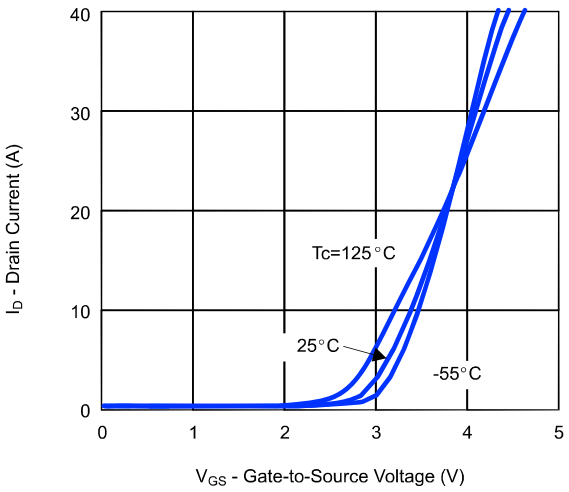
Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit		Min	Typ	Max	Unit
STATIC							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA V_{DS}=V_{GS}, I_D=-250μA	N-Ch P-Ch	1.0 -1.0	1.5 -1.5	3.0 -3.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V	N-Ch P-Ch			±100 ±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V V_{DS}=-30V, V_{GS}=0V	N-Ch P-Ch			1 -1	μA
		V_{DS}=30V, V_{GS}=0V,T_J=55℃ V_{DS}=-30V, V_{GS}=0V,T_J=55℃	N-Ch P-Ch			25 -25	
$I_{D(ON)}$	On-State Drain Current	V_{DS}≧5V, V_{GS}= 10V V_{DS}≦-5V, V_{GS}= -10V	N-Ch P-Ch	20 -20			A
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V, I_D= 6.9A V_{GS}=-10V, I_D= -6.1A	N-Ch P-Ch		21 30	25 35	mΩ
		V_{GS}=4.5V, I_D= 5.8A V_{GS}=-4.5V, I_D= -5.1A	N-Ch P-Ch		32 48	40 58	
V_{SD}	Diode Forward Voltage	I_S=1.7A, V_{GS}=0V I_S=-1.7A, V_{GS}=0V	N-Ch P-Ch		0.8 -0.8	1.2 -1.2	V
DYNAMIC							
Qg	Total Gate Charge	N-Channel V_{DS}=15V, V_{GS}=10V, I_D=6.9A P-Channel V_{DS}=-15V, V_{GS}=-10V, I_D=-6.1A	N-Ch P-Ch		12 21	15 25	nC
Qgs	Gate-Source Charge		N-Ch P-Ch		2 4		
Qgd	Gate-Drain Charge		N-Ch P-Ch		2.5 6		
Ciss	Input Capacitance	N-Channel V_{DS}=15V, V_{GS}=0V, f=1MHz P-Channel V_{DS}=15V, V_{GS}=0V, f=1MHz	N-Ch P-Ch		360 840	420 980	pF
Coss	Output Capacitance		N-Ch P-Ch		70 120		
Crss	Reverse Transfer Capacitance		N-Ch P-Ch		17 32		
Rg	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz	N-Ch P-Ch		0.5 6		Ω
$t_{d(on)}$	Turn-On Delay Time	N-Channel V_{DD}=15V, R_L =15Ω I_D=1A, V_{GEN}=10V, R_G=6Ω P-Channel V_{DD}=-15V, R_L =15Ω I_D=-1A, V_{GEN}=-10V,R_G=6Ω	N-Ch P-Ch		9.3 32	13 41	ns
t_r	Turn-On Rise Time		N-Ch P-Ch		14 13	18 17	
$t_{d(off)}$	Turn-Off Delay Time		N-Ch P-Ch		32 58	41 75	
t_f	Turn-Off Fall Time		N-Ch P-Ch		3.2 6.8	5 9	

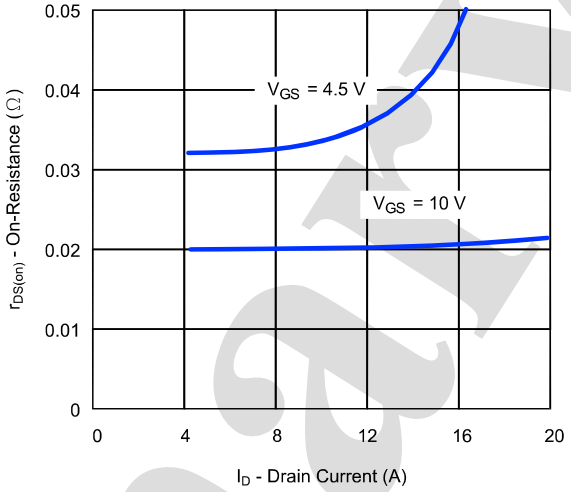
N- and P-Channel 30-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted) N-CHANNEL

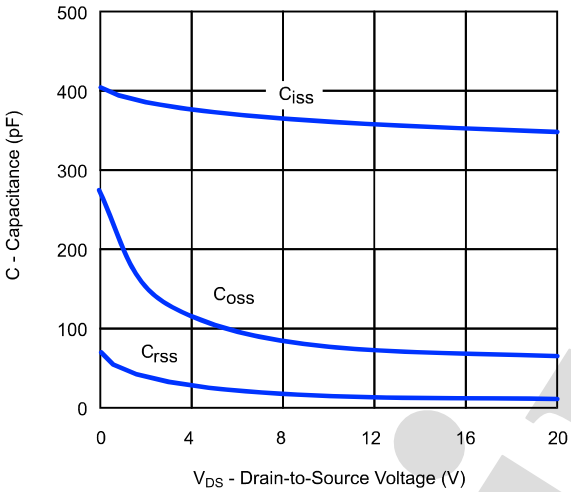
Transfer Characteristics



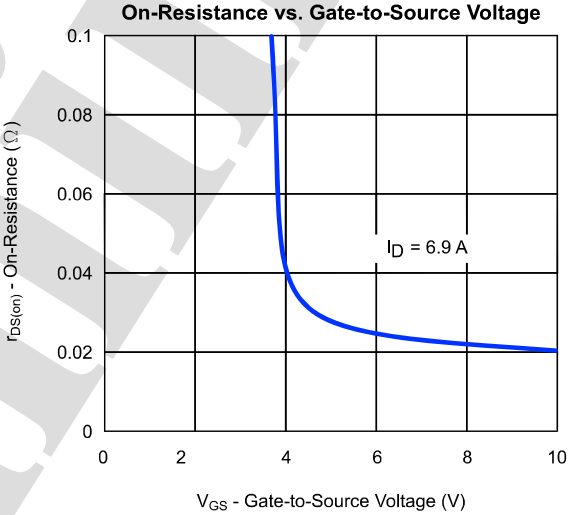
On-Resistance vs. Drain Current



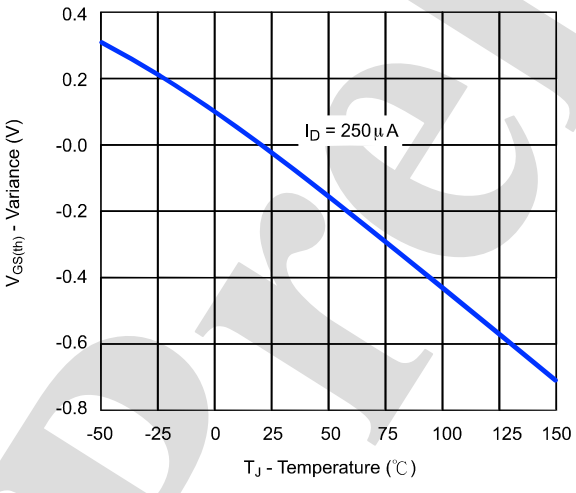
Capacitance



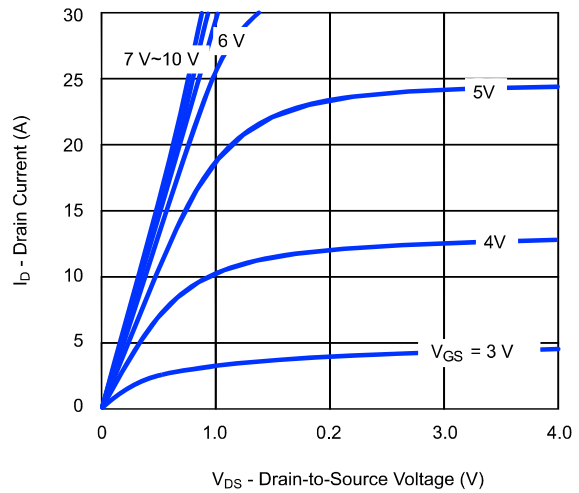
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



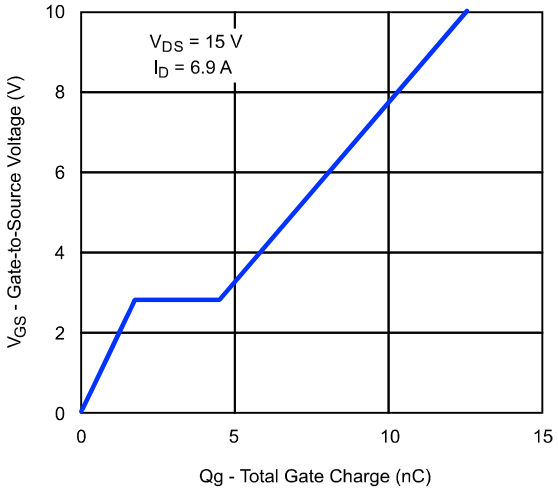
On-Region Characteristics



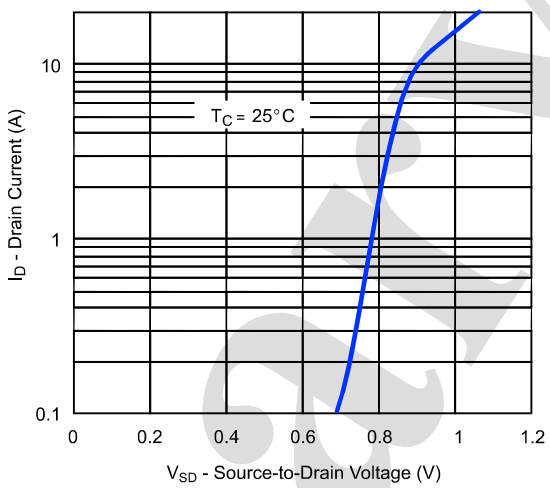
N- and P-Channel 30-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted) N-CHANNEL

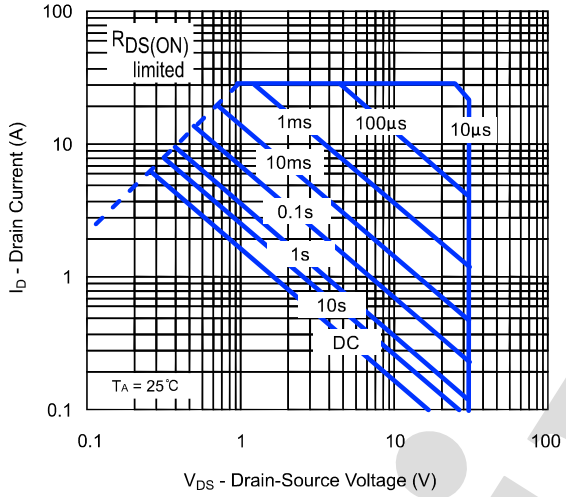
Gate Charge



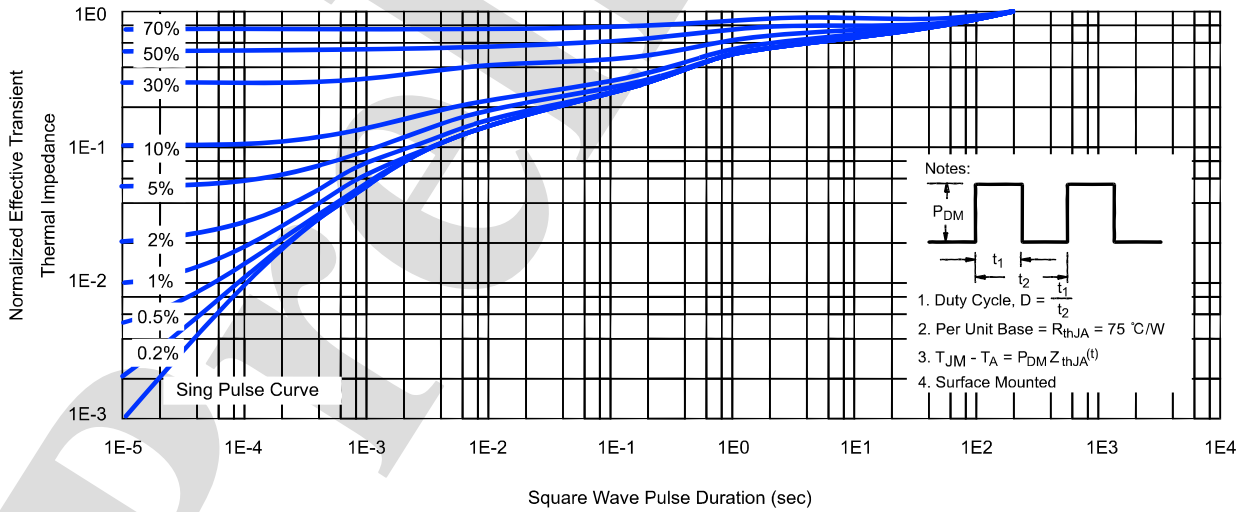
On-Resistance vs. Drain Current



Maximum Forward Biased Safe Operating Area



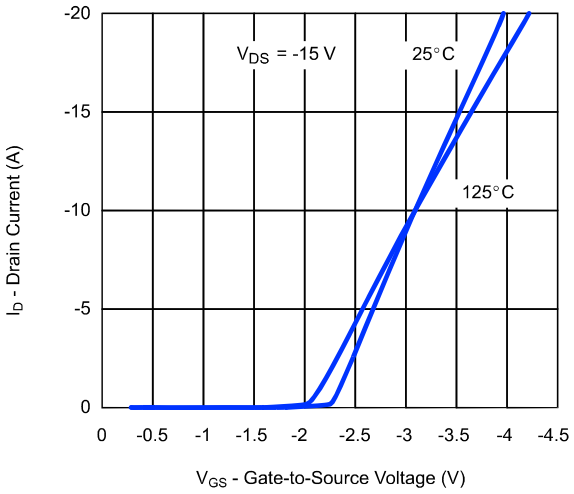
Normalized Thermal Transient Impedance, Junction-to-Ambient



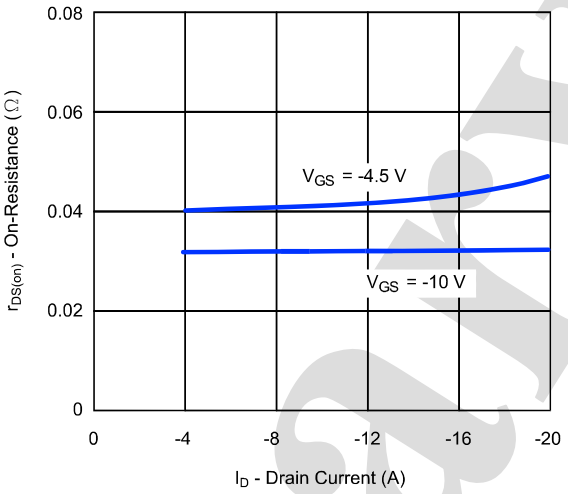
N- and P-Channel 30-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted) P-CHANNEL

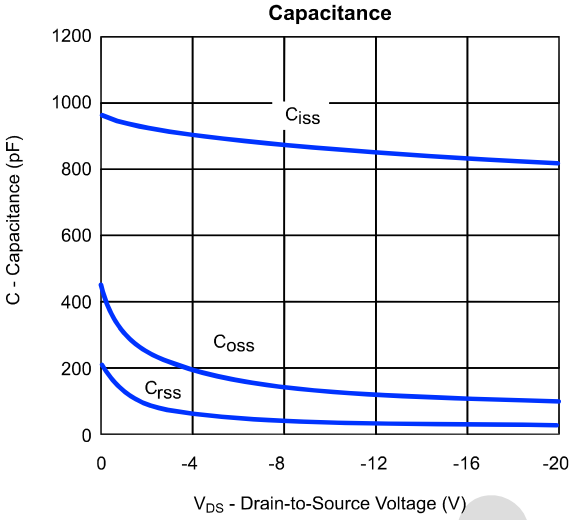
Transfer Characteristics



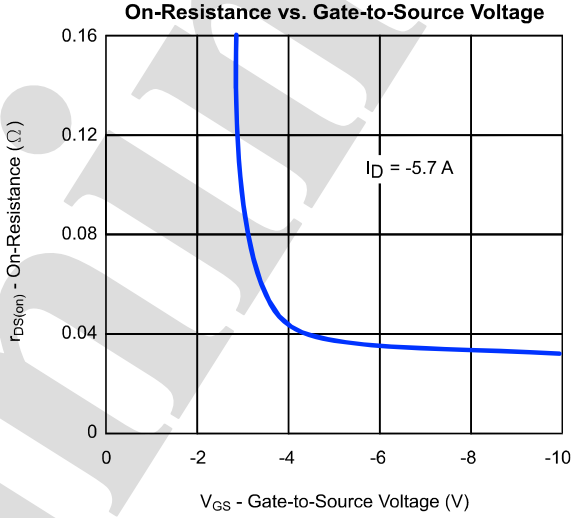
On-Resistance vs. Drain Current



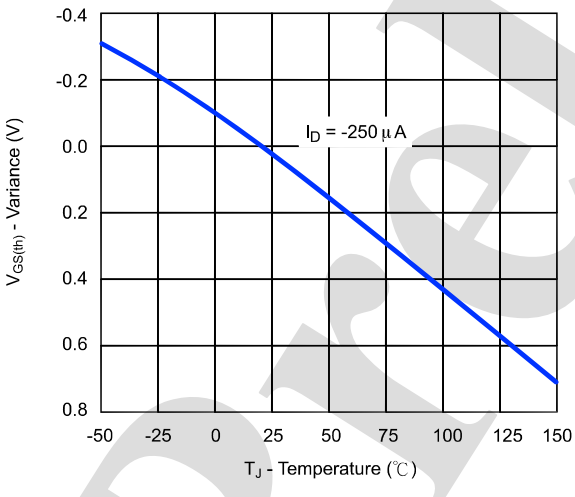
Capacitance



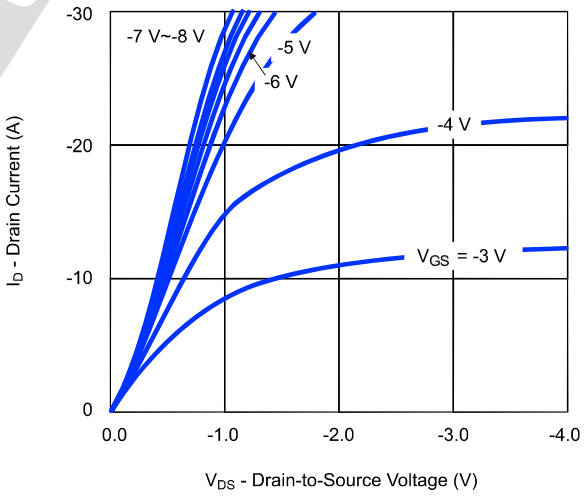
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



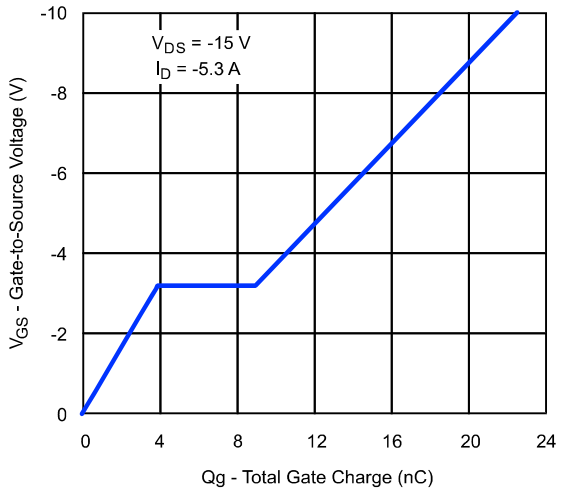
On-Region Characteristics



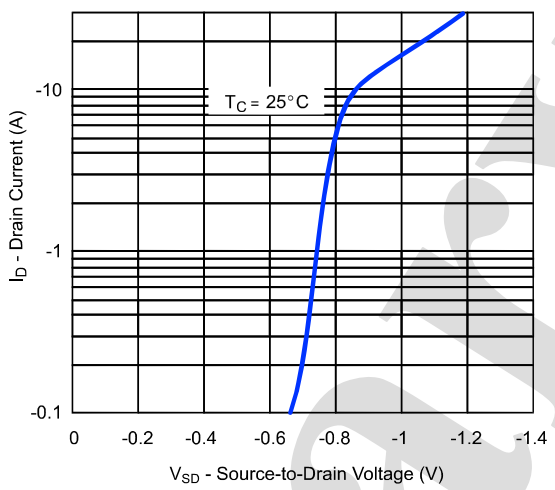
N- and P-Channel 30-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted) P-CHANNEL

Gate Charge



On-Resistance vs. Drain Current



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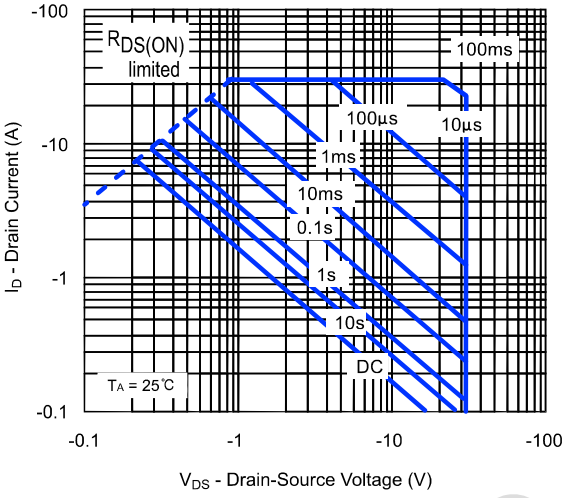
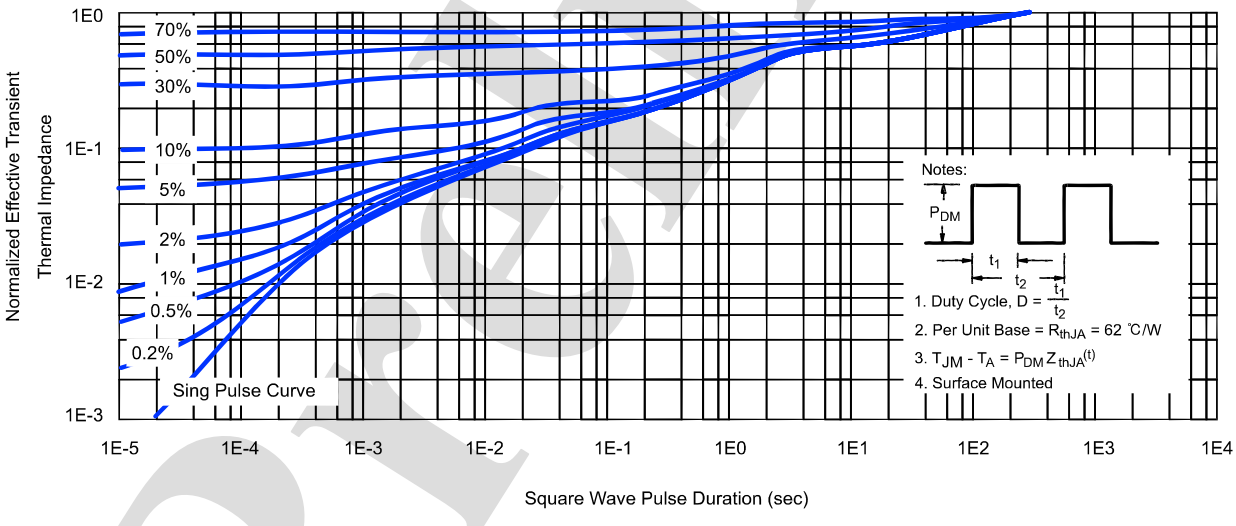
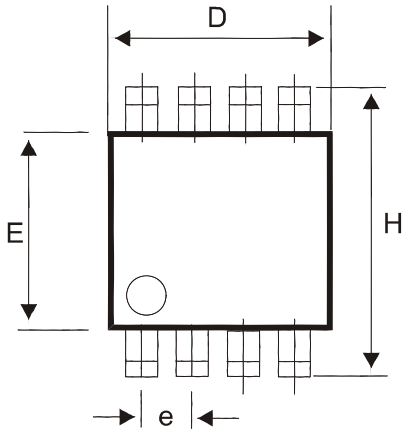
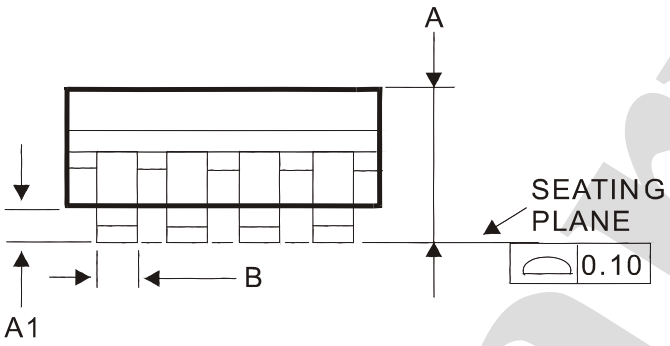


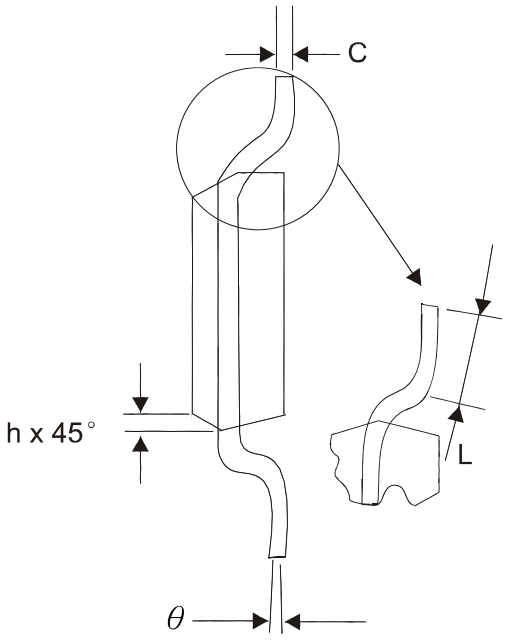
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOP-8 Package Outline







DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°